AMENDMENTS TO THE DRAWINGS

The attached sheet of drawings includes new Fig. 5. Support for new Fig. 5 is found in the original specification at paragraph 0026.

Attachment: New Drawing Sheet including new Fig. 5

REMARKS/ARGUMENTS

In the Office Action, the Examiner noted that claims 1-33 are pending in the application and claims 13-21 are withdrawn from consideration. The Examiner additionally stated that claims 1-12 and 22-33 are rejected. By this amendment, claims 3-4, 6-7, 10-24, 26, and 32 have been cancelled; claims 1-2, 5, 8-9, 25, 27-30, and 33 have been amended; and new claim 34 has been added. Hence, claims 1-2, 5, 8-9, 25, 27-31, and 33-34 are pending in the application.

Applicant hereby requests further examination and reconsideration of the application, in view of the foregoing amendments.

In the Specification

Applicant has amended the specification to secure a substantial correspondence between the claims amended herein and the remainder of the specification. Specifically, paragraph 0026 has been amended to make reference to new Fig. 5, which is supported in original paragraph 0026 of Applicants' specification. Additionally, Applicant has corrected the abstract as required by the Examiner. No new matter is presented.

In the Claims

Rejections Under 35 U.S.C. §112, second paragraph

The Examiner rejected claims 1-2 and 22-33 under 35 U.S.C. 112, second paragraph as being indefinite.

Applicants have amended claim 1 to change "carry" bits to "borrow" bits as suggested by the Examiner.

Applicants have canceled claims 3, 11-12 and 22.

Rejections Under 35 U.S.C. §101

The Examiner rejected claims 11-12 and 25-33 under 35 U.S.C. 101 as being directed to non-statutory subject matter.

Applicants have canceled claims 11-12.

Applicants have amended claim 25 to recite the further limitation of storing said result in a register of a microprocessor, which produces a useful, concrete, and tangible result.

Applicants have amended claim 33 to recite a computer program product embodied on a computer-readable storage medium for use with a computing device comprising a computer-readable storage medium, having computer-readable program code embodied in said medium for providing an apparatus for executing an MMX PSADBW instruction, which Applicants respectfully assert is statutory subject matter.

Rejections Under 35 U.S.C. §102(b) and Under 35 U.S.C. §103(a)

The Examiner rejected claims 1, 8-10 and 25-32 under 35 U.S.C. 102(b) as being clearly anticipated by Uratani et al., U.S. Patent No. 5,610,850 (hereinafter, *Uratani*). The Examiner rejected claims 11-12 and 33 under 35 U.S.C. 103(a) as being unpatentable over *Uratani*. The Examiner rejected claims 2-7 and 22-24 under 35 U.S.C. 103(a) as being unpatentable over *Uratani* in view of Abdallah et al., U.S. Patent No. 6,377,970 (hereinafter *Abdallah*).

With respect to amended claim 1, Applicants respectfully assert that neither *Uratani* nor *Abdallah* teach a first adder that adds selectively inverted differences of packed operands based on the values of borrow bits associated with the differences to generate a first sum and a first carry, and a second adder that adds borrow bits to generate a second sum and a second carry in parallel with the first adder generating the first sum and carry.

Abdallah teaches three different embodiments for performing the PSAD instruction shown in Figs. 5-7. However, none of the embodiments adds borrow bits of the generated differences, much less in parallel with the addition of selectively inverted packed differences with which the borrow bits are associated. The embodiments of Figs. 6 and 7 do not even teach generating the borrow bits, and the embodiment of Fig. 5 does not add the borrow bits (referred to as carry bits "C" by *Abdallah*); rather, the embodiment of Fig. 5 examines the carry bits to determine whether the PABSRC microinstruction should perform a two's-complement operation on the result of each respective difference "F".

Uratani teaches adding the borrow bits to the selectively inverted differences (see Figs. 13-15); however, *Uratani* does not teach a first adder that generates a first sum and a first carry from the selectively inverted differences, and a second adder that adds the associated borrow bits to generate a second sum and a second carry in parallel with the first adder generating the first sum and carry. Rather, *Uratani* teaches adding the first bits of the selectively inverted differences and borrow bits all together in a first bit adder which are all part of a Wallace tree adder that generates a single sum and carry. See Figs. 14-15.

Method claim 25 and computer program product claim 33 have been amended to include similar limitations to amended claim 1.

With respect to claims 2, 5, and 8-9, these claims depend from claim 1 and add further limitations that are neither anticipated nor made obvious by *Uratani* in view of *Abdallah*. Accordingly, Applicant respectfully requests that the Examiner withdraw his rejections to claims 2, 5, and 8-9.

With respect to claims 27-31 and 33-34, these claims depend from claim 25 and add further limitations that are neither anticipated nor made obvious by *Uratani* in view of *Abdallah*. Accordingly, Applicant respectfully requests that the Examiner withdraw his rejections to claims 27-31 and 33-34.

The limitations recited in new claim 34 are found in new Fig. 5.

CONCLUSIONS

In view of the arguments advance above, Applicant respectfully submits that claims 1-2, 5, 8-9, 25, 27-31, and 33-34 are in condition for allowance. Reconsideration of the rejections is requested, and allowance of the claims is solicited.

Applicant earnestly requests that the Examiner contact the undersigned practitioner by telephone if the Examiner has any questions or suggestions concerning this amendment, the application, or allowance of any claims thereof.

Respectfully submitted,

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By:_____

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07/30/2007

Date: _____

Attachment: New Drawing Sheet including new Fig. 5